WHAT IS CLAIMED IS:

1. A basic input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors.

2. The BIOS of claim 1 wherein one of the plurality of processors comprises a boot strap processor, the computer program instructions being operable to cause the boot strap processor to assign each of the different portions of the system memory to one of the selected processors.

3. The BIOS of claim 2 wherein the plurality of processors are configured in a plurality of processor clusters, each of the clusters corresponding to at least one of the different portions of the system memory, the computer program instructions being operable to cause the boot strap processor to assign each of the different portions of system memory to one of the selected processors in the corresponding cluster.

4. The BIOS of claim 3 wherein each of the processors in each of the clusters has one of the different portions of the system memory associated therewith, the computer program instructions being operable to cause the boot strap processor to assign each of the different portions of the system memory to its associated processor.

5. The BIOS of claim 3 wherein the computer program instructions are operable to cause the boot strap processor to assign only one of the processors in each cluster to the corresponding portion of the system memory.

6. The BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to instruct the selected processors to begin testing of the system memory.

7. The BIOS of claim 6 wherein the computer program instructions are operable to cause each of the selected processors to initialize and validate its assigned portion of the system memory.

8. The BIOS of claim 7 wherein the computer program instructions are operable to cause each of the selected processors to report memory testing progress to the boot strap processor.

9. The BIOS of claim 8 wherein the computer program instructions are operable to cause each of the selected processors to report the memory testing progress by writing to a field in shared memory associated with the boot strap processor.

10. The BIOS of claim 8 wherein the computer program instructions are operable to cause each of the selected processors to update the memory testing progress periodically.

11. The BIOS of claim 10 wherein the computer program instructions are operable to cause each of the selected processors to update the memory testing progress after testing a memory segment in its assigned portion of the system memory.

12. The BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to monitor progress in testing of the system memory by the selected processors.

13. The BIOS of claim 12 wherein the computer program instructions are operable to cause the boot strap processor to periodically update status information corresponding to the progress.

14. The BIOS of claim 13 wherein the computer program instructions are operable to cause the boot strap processor to update the status information after testing a memory segment in its assigned portion of the system memory.

15. The BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to generate memory testing results upon completion of the testing of the system memory by the selected processors.

16. The BIOS of claim 15 wherein the computer program instructions are operable to cause the boot strap processor to disable any memory modules corresponding to corrupted memory ranges indicated in the memory testing results.

17. The BIOS of claim 16 wherein the computer program instructions are operable to cause the computer system to reboot after disabling the memory modules.

18. The BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to allocate separate stack memory in a shared memory for each of the selected processors.

19. The BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to disable interrupt generation by the selected processors.

20. The BIOS of claim 2 wherein the computer program instructions are operable to associate a lock prefix with instructions targeting a shared memory associated with the boot strap processor thereby ensuring that two of the processors do not access the shared memory at the same time.

21. The BIOS of claim 1 wherein the computer system comprises a plurality of point-to-point links interconnecting the plurality of processors, the computer program instructions being operable to facilitate testing of the memory via the point-to-point links.

22. The BIOS of claim 21 wherein the plurality of processors are configured in a plurality of clusters, and the point-to-point links comprise intra-cluster point-to-point links interconnecting the processors within each cluster and inter-cluster point-to-point links interconnecting the clusters.

23. The BIOS of claim 1 wherein the computer system comprises a bus for interconnecting the plurality of processors and the system memory, the computer program instructions being operable to facilitate testing of the memory via the bus.

24. A computer system comprising a plurality of processors, a system memory, and a basic input/output system (BIOS) embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors.

25. The computer system of claim 24 further comprising a plurality of point-to-point links interconnecting the plurality of processors.

26. The computer system of claim 25 wherein the plurality of processors are configured in a plurality of clusters, and the point-to-point links comprise intra-cluster point-to-point links interconnecting the processors within each cluster and inter-cluster point-to-point links interconnecting the clusters.

27. The computer system of claim 24 further comprising a bus for interconnecting the plurality of processors and the system memory.

28. A basic input/output system (BIOS) for use in a computer system having a plurality of processors, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous operation of selected ones of the plurality of processors.

29. The BIOS of claim 28 wherein the computer system also comprises system memory, the computer program instructions being operable to facilitate substantially simultaneous testing of different portions of the system memory by the selected processors.

30. A computer system comprising a plurality of processors and a basic input/output system (BIOS) embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous operation of selected ones of the plurality of processors.

31. The computer system of claim 30 further comprising a plurality of point-to-point links interconnecting the plurality of processors.

32. The computer system of claim 31 wherein the plurality of processors are configured in a plurality of clusters, and the point-to-point links comprise intra-cluster point-to-point links interconnecting the processors within each cluster and inter-cluster point-to-point links interconnecting the clusters.

33. The computer system of claim 30 further comprising a bus for interconnecting the plurality of processors.